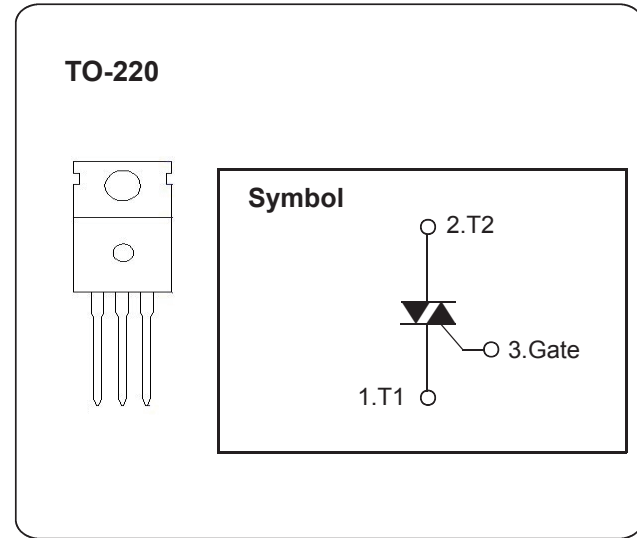


Bi-Directional Triode Thyristor

- High current density due to double mesa technology, SIPOS and Glass passivation .
BT25 series triacs is suitable for general purpose AC switching. They can be used as an ON/OFF function in applications such as static relays, heating regulation, induction motor starting circuits or phase control operation light dimmers, motor speed controllers.
- BT25 series are 3 Quadrants triacs, They are specially recommended for use on inductive loads.



Features

- Blocking Voltage to 600~ 800 V
- On- State Current Rating of 20A RMS at 90°C
- Uniform Gate Trigger Currents in Three Quadrants
- High Immunity to dV/dt- 1500V/us minimum at 125 °C
- Minimizes Snubber Networks for Protection
- Industry Standard TO- 220 Package
- High Commutating dI/dt- 4.0A/ms minimum at 125 °C
- Internally Isolated (2500VRMS)
- These are Pb- Free Devices

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Storage junction temperature range		Tstg	-40 to +150	°C
Operating junction temperature range		Tj	-40 to + 150	°C
Repetitive Peak OFF-state Voltage	Tj=25°C	V _{DRM}	600 and 800	V
Repetitive Peak Reverse Voltage	Tj=25°C	V _{RRM}	600 and 800	V
Non repetitive surge peak off-state voltage	Tp=10ms, Tj=25°C	V _{DSM}	700 and 900	V
Non repetitive peak reverse voltage		V _{RSM}	700 and 900	V
RMS on-state current(full sine wave)	TC=90°C	IT(RMS)	25	A
	TC=70°C			
Non repetitive surge peak on-state current (full cycle, Tj=25°C)	f=60Hz, t=16.7ms	ITSM	250	A
	f=50Hz, t=20ms		260	
I ² t Value for fusing	Tp=10ms	I ² t	340	A ² s
Critical rate of rise of on-state current IG=2*IGT, tr≤100ns, f=120Hz, Tj=125°C		dI/dt	50	A/us
Peak gate current(tp=20us, Tj=125°C)		I _{GM}	4	A
Peak gate power dissipation(tp=20us, Tj=125°C)		P _{GM}	10	W
Average gate power dissipation(Tj=125°C)		PG(AV)	1	W

Electrical Characteristics (T_j=25°C, unless other wise specified)

Symbol	Test Condition	Quadrant		Limit	Unit
I _{GT}	V _D =12V, R _L =33Ω	I - II -III	MAX	35	mA
V _{GT}		I - II -III	MAX	1.3	V
V _{GD}	V _D =V _{DRM} R _L =3.3KΩ T _j =125°C	I - II -III	MIN	0.2	V
I _L	I _G =1.2I _{GT}	I -III	MAX	50	mA
		II	MAX	60	mA
I _H	I _T =100mA		MAX	40	mA
Dv/dt	V _D =67%V _{DRM} gate open T _J =125°C		MIN	500	V/us
(Dv/dt) _c	(dl/dt) _c =8.8A/ms T _j =125°C		MIN	8.5	V/us

Static Characteristics

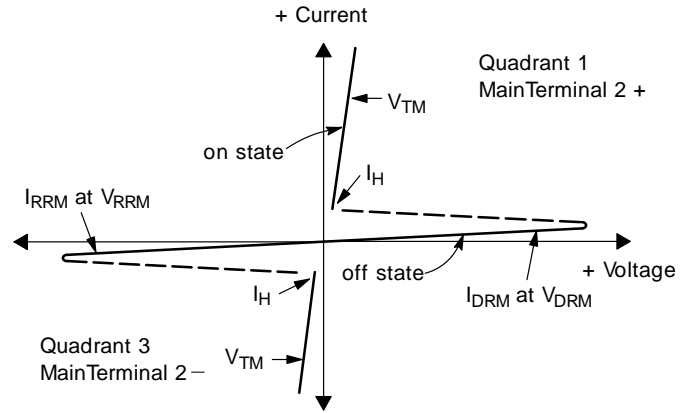
Symbol	Parameter		Value(MAX)	Unit
V _{TM}	ITM=35A, tp=380us	T _j =25°C	1.55	V
I _{DRM}	V _D =V _{DRM} V _R =V _{RDM}	T _j =25°C	5	uA
I _{RDM}		T _j =150°C	3	mA

Thermal Resistances

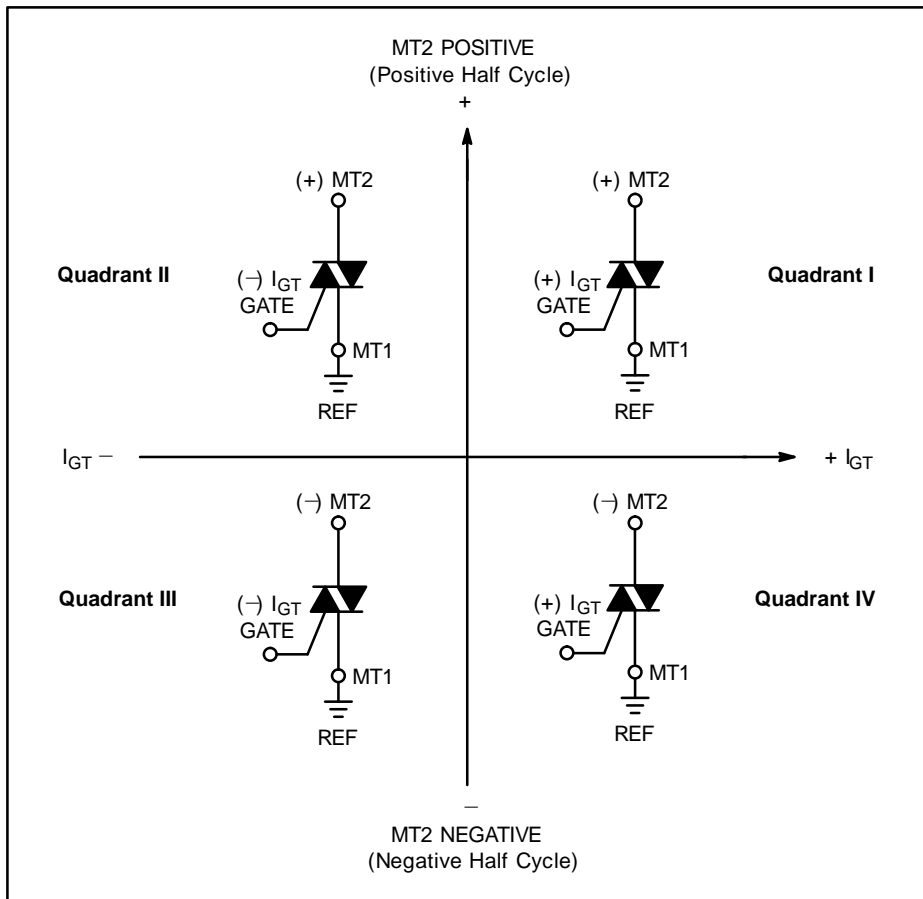
Symbol	Parameter	Value	Unit
R _{th} (J-C)	Junction to case(AC)	1.7	°C/W

Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All polarities are referenced to MT1.
 With in-phase signals (using standard AC lines) quadrants I and III are used.

Figure 1. Maximum power dissipation versus RMS on-state current (full cycle)

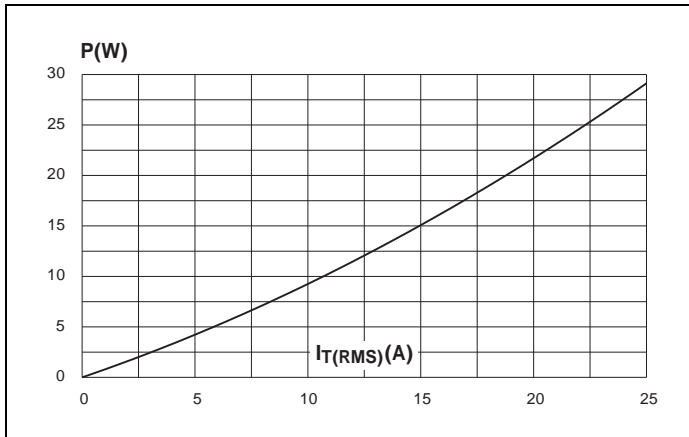


Figure 2. RMS on-state current versus case temperature (full cycle)

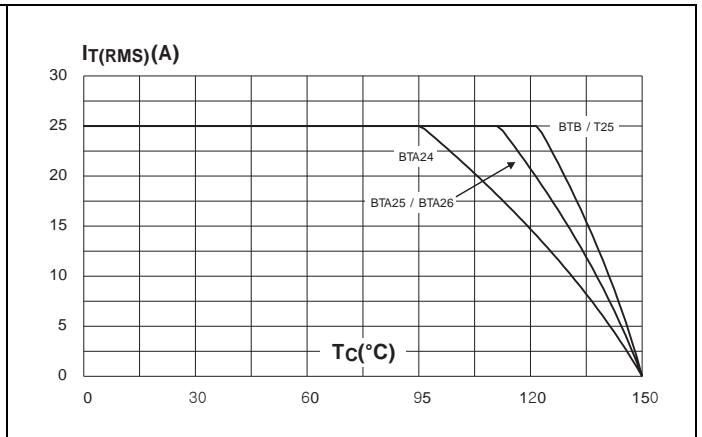


Figure 3. D²PAK RMS on-state current versus ambient temperature (printed circuit board FR4, copper thickness: 35µm) (full cycle)

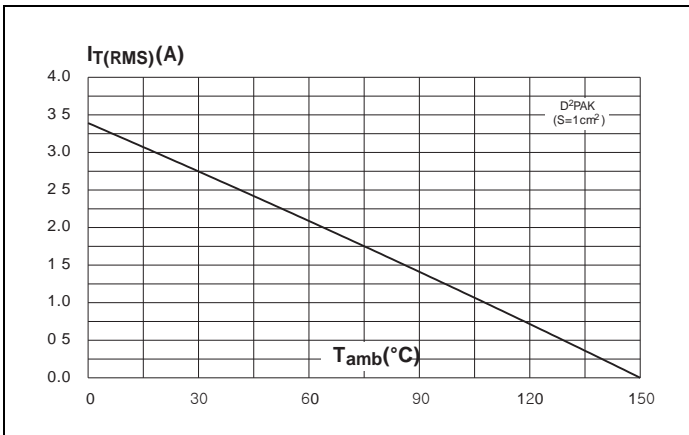


Figure 4. Relative variation of thermal impedance versus pulse duration

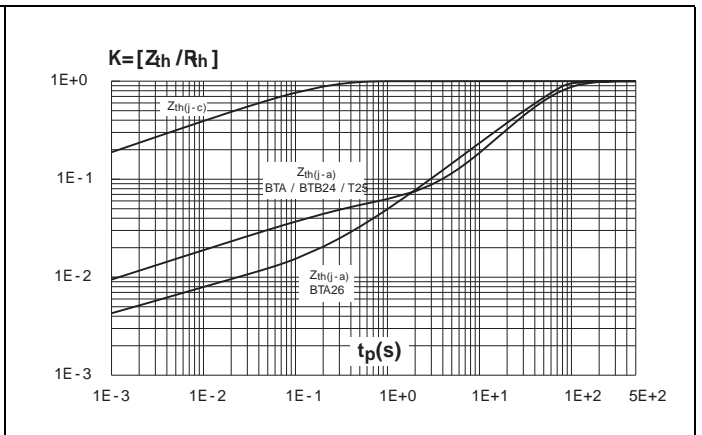


Figure 5. On-state characteristics (maximum values)

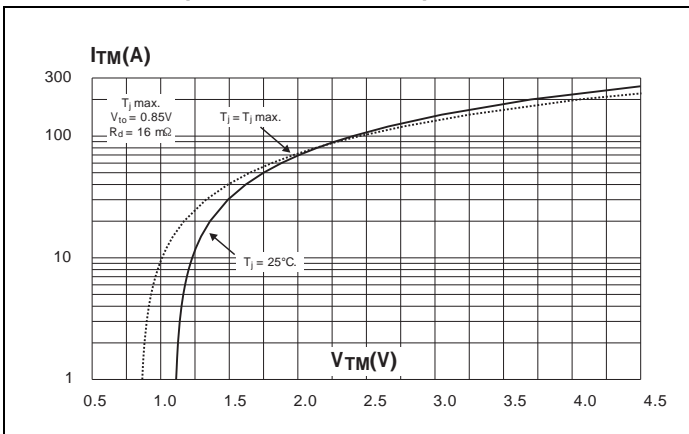


Figure 6. Surge peak on-state current versus number of cycles

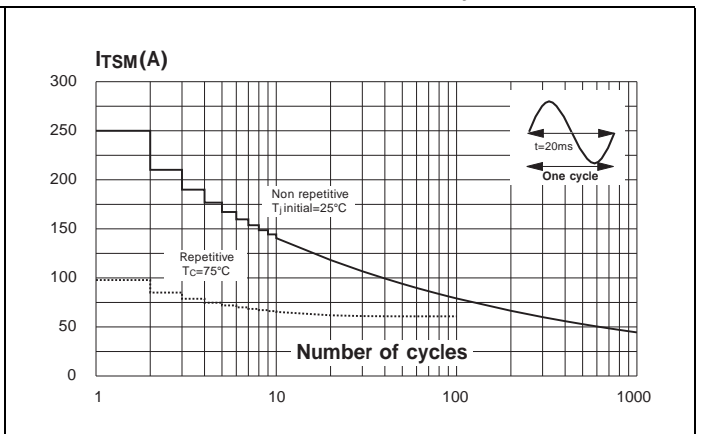


Figure 7. Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10$ ms and corresponding value of I^2t

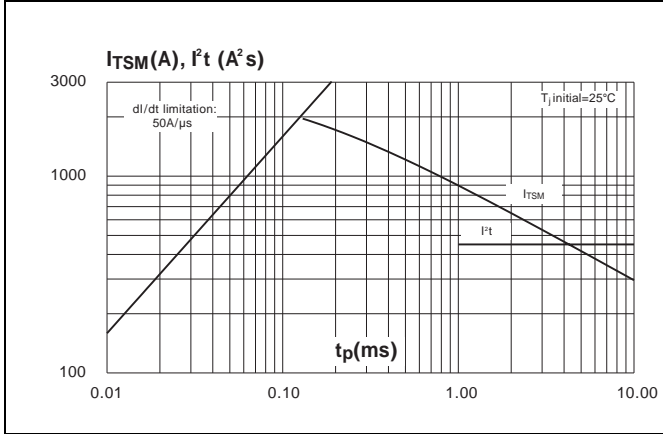


Figure 8. Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values)

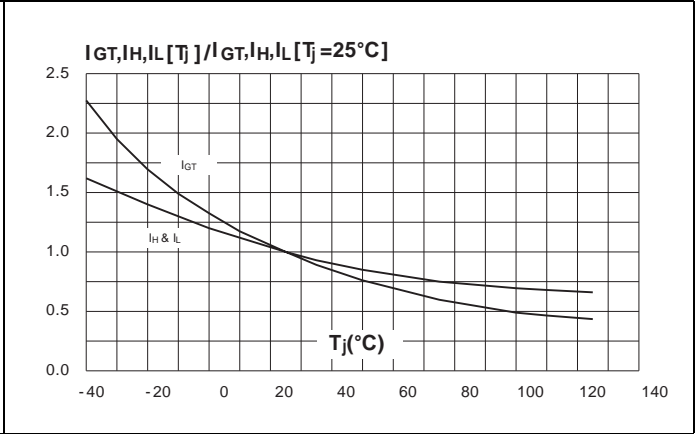


Figure 9. Relative variation of critical rate of decrease of main current versus $(dV/dt)_c$ (typical values)

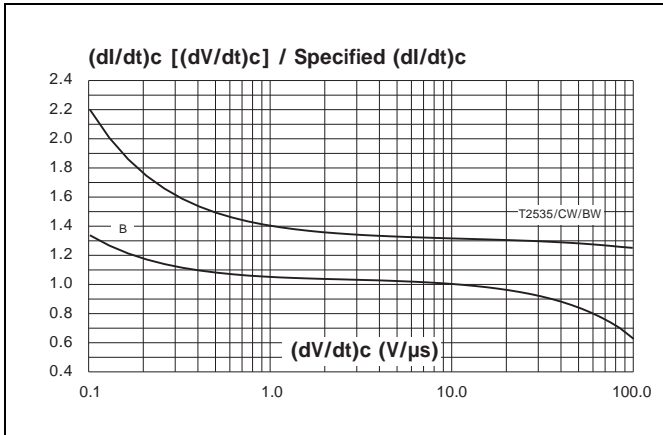


Figure 10. Relative variation of critical rate of decrease of main current versus $(dV/dt)_c$

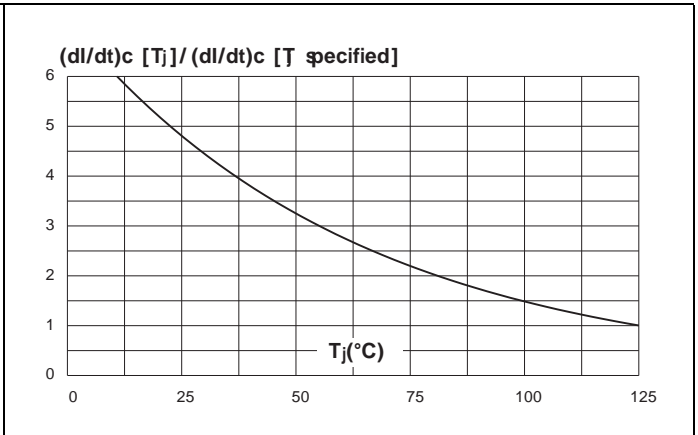


Figure 11. D²PAK Thermal resistance junction to ambient versus copper surface under tab (printed circuit board FR4, copper thickness: 35 μm)

